REMARKS

The claims are claims 1 to 8.

The application has been amended at several places. These amendments correct non-standard symbols which were originally printed incorrectly. The paragraph spanning pages 65 and 66 has been amended to refer to Figure 9 rather than Figure 17 and to include the reference numbers of Figure 9 in the 400's rather than the original reference numbers in the 300's.

Claims 1, 4, 6 and 8 are amended. Claims 1 and 6 have been amended to correct the article "an" to "a." This merely corrects an error in language. Claims 1 and 6 have been further amended to recite that sections not generating a carry output during the adding are passed unchanged into the saturated sum data word. As a result of this amendment, the term "saturated sum data word" is defined to have all sections that are 1's for sections generating a carry in the adding and sections that are unchanged otherwise. Thus the term "saturated sum data word" does not mean that all sections are saturated, but only those sections having an overflow (carry output) during the adding. Claim 4 is amended to make clear that the predetermined number of bits is the predetermined number of least significant bits of the truncating step in base claim 1. Claim 8 has been amended to change "to" to "for" to provide a better fit to the later recited "truncating."

Claims 1 to 8 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The OFFICE ACTION states that claim 1 recites "3 sequential steps of addition, saturation and truncation, however the specification discloses only a simultaneous operation of the three steps (pages 68-70)." The OFFICE ACTION then states these sequential process steps are not understood and the application is not considered enabling.

The Applicant respectfully submits that the original application includes a written description that enables the recitations of claim 1. The application states at page 68, lines 3 to 6:

> "Assume that the input data signal is 8 bits and that four such input data signals are packed into a single 32-bit memory word. Dithering of these four packed input data signals can be performed simultaneously."

This disclosure states that dithering occurs simultaneously for fro input data signals packed into a single 32-bit memory word. This disclosure does not state that the steps of this dithering takes place simultaneously. The application at page 68, line 6 to page 70, line 12 then describes the three steps in terms that require them to be sequential. The application states at page 68, lines 6 and 7 "The first step of this dithering process..." This implies that there are plural steps in "this dithering process." The application then lists three numbered equations (1 at page 68, lines 11 and 12; 2 at page 68, lines 28 and 29; and 3 at page 69, lines 20 and 21). The second and third steps require input from the prior step. The first step yields a result "X". The second step uses this prior result "X" as an input. The second step yields a result "Y". This third step uses this prior result "Y" as an input. These factors lead to a clear implication that the three steps are sequential.

The application does not state that these three steps are simultaneous. As noted above, the application states that the dithering can take place on four packed input data signals simultaneously. Both independent claims 1 and 6 recite this packing and the operation of the three steps on the packed data simultaneously. However, the application does not state that the three steps occur simultaneously. Note that the OFFICE ACTION

fails to point out the language in the application that requires "simultaneous operation of the three steps." On the contrary, the portions noted above strongly imply sequential operation. Accordingly, the invention of claims 1 to 8 is adequately described in the original application.

Claims 1 to 8 were further rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The OFFICE ACTION states that "There is a lack of written description for truncation of saturated components" as recited in claim 1. The OFFICE ACTION states at page 3, lines 1 to 3:

> "Claim 1 describes truncation of saturated sum data words, however the Specification only discusses the truncation to be preformed when saturation does not occur."

Thus the Examiner has ruled the written description fails to enable the truncation recited in claim 1.

The Applicant respectfully submits that the Examiner is in error regarding the teaching of the description. The application states at page 69, lines 12 to 15:

> "This saturation step can be skipped if the input is guaranteed not to exceed the binary number 1111.0000 in the 4Q4 format."

This part of the application states that the saturation step is optional. This part of the application states that the saturation step "can be skipped" if the sum "is guaranteed not to exceed" a stated amount. The Applicant respectfully submits that the stated amount "1111.0000" is less than the saturation amount of "1111.1111." Thus this portion of the application teaches the saturation step can be skipped if it is not needed. In contrast, this application fails to state any conditional operation of the

truncation step 3, described in the application from page 69, line 20 to page 70, line 8. Thus the application teaches the truncation always occurs.

Independent claims 1 and 6 each recite "saturating any section of said sum data word generating a carry output during said adding to a section of all 1's and passing other sections unchanged thereby forming a saturated sum data word." The Applicant respectfully submits that under the condition noted at page 69, lines 13 to 15 "if the input is guaranteed not to exceed the binary number 1111.0000 in the 4Q4 format," the sum did not generate a carry output. Thus the unconditional truncation recited in claims 1 and 6 corresponds to the invention described in the application.

Claims 1 to 5 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Ulichney U.S. Patent No. 5,912,745 and Balmer et al U.S. Patent No. 5,606,677. The OFFICE ACTION states that Ulichney teaches all the steps except for the selectively splittable ALU disclosed in Balmer et al.

Claim 1 recites subject matter not made obvious by the combination of Ulichney and Balmer et al. Claim 1 recites "saturating any section of said sum data word generating a carry output during said adding to a section of all 1's and passing other sections unchanged thereby forming a saturated sum data word." The Applicant respectfully submits that Ulichney fails to teach this claimed saturation. The OFFICE ACTION states at page 3, line 21 to page 4, line 1:

> "Ulichney further discloses a saturated coded sum word in column 10, Equation Set II. Saturation occurs when the weighted value is added to the pixel value for each element in the pattern array, which has its own particular value."

Ulichney states at column 10, lines 22 to 25:

"Referring again to FIG. 5, the cluster filter 60 and void filter 70 can be implemented by applying a modified convolution calculation to obtain a filter result F(x,y) for each bit element at each x,y location of the pattern array 32."

This portion of Ulichney states that filter result F(x,y) is the result of cluster filter 60 and void filter 70. Figure 5 illustrates that cluster filter 60 and void filter 70 are parts of void and cluster template generator 20, also illustrated in Figure 3. Figure 3 shows void and cluster template generator 20 produces dither template 22 and that dither system data generator 24 produces dither matrix 24a. Figure 4 shows adder 26 adds input pixel 13b to "normalized threshold on line 25a" (column 8, line 31). Note that Equation Set II shows F(x,y) as the result of the equation. Thus this is clearly not saturation on the sum data word recited in claim 1. The Applicant submits that the Equation Set II cited in the OFFICE ACTION is part of "defining a dither value" of Ulichney and not a part of the recited saturating of the sum data word. Note particularly the portion of Ulichney cited in the OFFICE ACTION does not include any reference to saturation or saturating. Thus the OFFICE ACTION states that Ulichney teaches saturation but fails to cite a portion of Ulichney which so teaches. The Applicant respectfully submits that Ulichney includes no teaching of saturation. Accordingly, claims 1 to 5 are allowable over the combination of Ulichney and Balmer et al.

Claim 1 recites further subject matter not made obvious by the combination of Ulichney and Balmer et al. Claim 1 recites "truncating a predetermined number of least significant bits of each section of said saturated sum data word forming a dither screen data word." Applicant respectfully submits that Ulichney fails to teach this claimed truncation. The OFFICE ACTION states at page 4, lines 1 to 3:

> "Referring now to Figure 8, Ulichney discloses truncation of the summed code word in column 12, lines 11-13. As described, a predetermined number of minority bits are removed, forming the output image word."

Ulichney states at column 11, lines 58 to 62:

> "Referring now to FIG. 8, a flow diagram displaying the logical operation of an embodiment of the binary pattern processor 50 of FIG. 5 is shown, and will be described with references to FIGS. 5, 9 and 10, the latter two figures depicting typical outputs of the binary pattern processor 50."

The portion of column 12 of Ulichney cited in the OFFICE ACTION refers to step 103 of the flow diagram of Figure 8. Figure 5 illustrates binary bit processor 50 as a part of void and cluster template generator 20, also illustrated in Figure 3. Figure 3 shows void and cluster template generator 20 produces dither template 22 and that dither system data generator 24 produces dither matrix 24a. Figure 4 shows adder 26 adds input pixel 13b to "normalized threshold on line 25a" (column 8, line 31). Thus the portion of Ulichney cited in the OFFICE ACTION does not deal with processing pixel data but with the "defining a dither value" of Ulichney. This portion of Ulichney fails to teach that this "truncation" is of the saturated value from Equation Set II as required by the above quoted recitations of claim 1. That is, the two portions of Ulichney cited in the OFFICE ACTION fail to cooperate as recited in claim 1. Note further that the portion of Ulichney cited in the OFFICE ACTION does not include any reference to truncation or truncating. The OFFICE ACTION fails to state how the disclosed removal of a predetermined number of minority bits amounts to the claimed truncation. The Applicant respectfully submits that Ulichney includes no teaching of truncation. Accordingly, claims 1 to 5 are allowable over the combination of Ulichney and Balmer et al.

Claim 3 recites subject matter not made obvious by the combination of Ulichney and Balmer et al. Claim 3 recites "right shifting," forming a mask data word" and "forming a logical ADN." The OFFICE ACTION cites no portion of Ulichney or Balmer et al as allegedly making obvious these steps. The portion of Ulichney cited in the OFFICE ACTION includes no mention of any of these steps. The OFFICE ACTION implies that Ulichney teaches truncating and therefore must make obvious all forms of truncating. The Applicant respectfully submits this implication is clearly erroneous. Since the cited portion of Ulichney includes no teaching of these steps recited in claim 3, claim 3 is not made obvious by the combination of Ulichney and Balmer et al.

Claims 6, 7 and 8 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Ulichney U.S. Patent No. 5,912,745, Balmer et al U.S. Patent No. 5,606,677 and Taggart U.S. Patent No. 5,687,087. This rejection is similar to the rejection of claims 1 to 5 with Taggart added for its teaching of a printer.

Claim 6 recites subject matter not made obvious by the combination of Ulichney, Balmer et al and Taggart. Claim 6 recites "saturating any section of said sum data word generating a carry output during said adding to a section of all 1's and passing other sections unchanged thereby forming a saturated sum data word." The Applicant respectfully submits that Ulichney fails to teach this claimed saturation. The reasons are the same as argued above with respect to claim 1. Equation Set II cited in the OFFICE ACTION is part of "defining a dither value" of Ulichney and not a part of the recited saturating of the sum data word. Ulichney does not include any reference to saturation or saturating. Accordingly, claims 6 to 8 are allowable over the combination of Ulichney, Balmer et al and Taggart.

Claim 6 recites further subject matter not made obvious by the combination of Ulichney, Balmer et al and Taggart. Claim 6 recites

"truncating a predetermined number of least significant bits of each section of said saturated sum data word forming a dither screen data word." The portion of Ulichney cited in the OFFICE ACTION does not deal with processing pixel data but with the "defining a dither value" of Ulichney. This portion of Ulichney fails to teach that this "truncation" is of the saturated value from Equation Set II as required by the above quoted recitations of claim 6. That is, the two portions of Ulichney cited in the OFFICE ACTION fail to cooperate as recited in claim 6. Ulichney does not include any reference to truncation or truncating. Accordingly, claims 6 to 8 are allowable over the combination of Ulichney, Balmer et al and Taggart.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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